REMARKS

Claims 1-18 are pending in the present application. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102, Anticipation, Claims 1-4, 7-14, and 17-18

The examiner has rejected claims 1-4, 7-14, and 17-18 under 35 U.S.C. § 102 as anticipated by *Monzel III* et al., U.S. Patent No. 6,864,716 (hereinafter "*Monzel*"). This rejection is respectfully traversed.

As to claim 1, the examiner states:

> Referring to claim 1, Monzel discloses a method for providing a metal programmable device, the method comprising:
> providing an array of programmable cells (Claim 1, step 1);
> providing an array of pre-diffused memory cells (Claim 1 step 2);
> providing a plurality of memory interface control blocks, wherein each memory interface control block accesses the pre-diffused memory cells as a different memory type (in Abstract; Fig. 3E, col. 4, lines 23-50, Monzel discloses a plurality of peripheral logic blocks ("memory interface control block") may be used to configured to access the core memory cell as various memory types); and
> connecting a first memory interface control block from within the plurality of memory interface control blocks to a first portion of the memory cells (in Fig. 3C, col. 3 lines 45-47, Monzel discloses the peripheral logic within 324, "a first memory interface control block", is configured/connected to access memory 1), wherein logic within the array of programmable cells accesses at least a first portion of the array of pre-diffused memory cells as a first memory type using the first memory interface control block (in Fig. 3C, col. 3, lines 35+, Monzel discloses some/all of logic of element 324 ("a first memory interface control block") accesses a first portion of memory core).

Office Action dated November 14, 2005, pages 2-3.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the

reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Claim 1 is as follows:

> 1. A method for providing a metal programmable device, the method comprising:
> providing an array of programmable cells;
> providing an array of pre-diffused memory cells;
> providing a plurality of memory interface control blocks, wherein each memory interface control block accesses the pre-diffused memory cells as a different memory type; and
> connecting a first memory interface control block from within the plurality of memory interface control blocks to a first portion of the memory cells, wherein logic within the array of programmable cells accesses at least a first portion of the array of pre-diffused memory cells as a first memory type using the first memory interface control block.

Monzel fails to teach the claimed feature of "providing a plurality of memory interface control blocks, wherein each memory interface control block accesses the pre-diffused memory cells as a different memory type". The examiner asserts otherwise, citing from the Abstract and col. 4, lines 23-50 of *Monzel*. Each of these portions of *Monzel* are discussed in turn in order to show that the examiner's assertions are mistaken. *Monzel's* Abstract is as follows (emphasis added):

> A pre-diffused high density array of core memory cells is provided in a metal programmable device. *The peripheral logic is made up of gate array cells in the metal programmable device.* The peripheral logic may be configured to access the core memory cells as various memory types, widths, depths, and other configurations. If the entire memory is not needed, then the unused memory cells can be used as logic gates. The application-specific circuit, including peripheral logic, memory interface logic, and memory configuration is programmed with a metal layer.

Here, *Monzel* states that the "peripheral logic is made up of gate array cells in the metal programmable device" and "[t]the peripheral logic may be configured to access the core memory cells". However, neither this portion of *Monzel* nor any other portion of *Monzel* teaches a plurality of memory interface control blocks that is distinct from the array of programmable cells because, in *Monzel*, the peripheral logic that accesses the core memory cells is made up of gate array cells. *Monzel* teaches a metal programmable device with (1) gate array cells and (2) core

memory cells. *Monzel* teaches that *the peripheral logic used to access the core memory cells is made up of gate array cells.*

In contrast, claim 1 of the present invention recites a metal programmable device with (1) an array of programmable cells, (2) an array of pre-diffused memory cells, and (3) a plurality of memory interface control blocks, wherein each memory interface control block accesses the pre-diffused memory cells. *Monzel* does not teach a distinct plurality of memory interface control blocks which access the pre-diffused memory cells, because in *Monzel*, the peripheral logic that accesses the core memory cells is made up of gate array cells. *Monzel's* Abstract therefore fails to teach the claimed feature of "providing a plurality of memory interface control blocks, wherein each memory interface control block accesses the pre-diffused memory cells as a different memory type".

Nevertheless, the examiner also asserts that other portions of Monzel teach the claimed feature. Specifically, the examiner refers to the following portion of *Monzel*:

> Turning to **FIG. 3E**, metal programmable device **340** includes *memory core* **345**, *gate array cells* **342**, gate array cells **344**, gate array cells **346**, and gate array cells **348**. *Some or all of the logic made up of gate array cells 342 accesses a first portion of the memory core*, shown as "memory 1," as a dual port memory with one read port and one write port. Some or all of the logic made up of gate array cells **344** accesses a second portion of the memory core, shown as "memory 2," as a dual port memory with one read port and one write port. Some or all of the logic made up of gate array cells **346** accesses a second portion of the memory core, shown as "memory 3," as a single port memory with one read port and one write port. Some or all of the logic made up of gate array cells **348** accesses a second portion of the memory core, shown as "memory 4," as a dual port memory with two read ports and two write ports.
>
> In this example, the same memory core is capable of providing two 211 memory portions, a 111 memory portion, and a 222 memory portion. The same metal programmable device can be programmed with the customer logic and specialized memory configurations based on need, simply by applying the appropriate metal layer. A common memory core cell is an eight-transistor dual port core cell. However, there are many possible techniques for creating a dual port memory core cell. The configurable memory may also use other types of dual port core cells within the scope of the present invention.

Monzel, col. 4, lines 23-50 (emphasis added).

Again, *Monzel* teaches that the metal programmable device includes (1) gate array cells

and (2) a memory core. *Monzel* also teaches that the *logic which accesses the memory core is made up of gate array cells*. In contrast, claim 1 of the present invention recites a metal programmable device with (1) an array of programmable cells, (2) an array of pre-diffused memory cells, and (3) a plurality of memory interface control blocks, wherein each memory interface control block accesses the pre-diffused memory cells. *Monzel* does not teach a distinct plurality of memory interface control blocks which access the pre-diffused memory cells, because in *Monzel*, the metal programmable device has a memory core and gate array cells and *the peripheral logic that accesses the core memory cells is made up of gate array cells*. The cited portion of *Monzel* therefore fails to teach the claimed feature of "providing a plurality of memory interface control blocks, wherein each memory interface control block accesses the pre-diffused memory cells as a different memory type".

Thus in *Monzel*, neither the Abstract nor Fig. 3E, col. 4, lines 23-50 teach the claimed feature of "providing a plurality of memory interface control blocks, wherein each memory interface control block accesses the pre-diffused memory cells as a different memory type". Additionally, *Monzel* does not elsewhere teach these claimed features. Because *Monzel* does not teach all the features of claim 1, *Monzel* does not anticipate claim 1.

Because claims 2-8 depend from claim 1, the same distinctions between *Monzel* and the invention of claim 1 can be made for these claims. Additionally, claims 2-8 claim other additional combinations of features not suggested by the reference. Consequently, Applicants respectfully urge that the rejection of claims 1-8 has been overcome.

Claims 9-18 claim a metal programmable device implementing the methods of claims 1-8. Therefore, the same distinctions between *Monzel* and the inventions of claims 1-8 can be made for claims 9-18. Consequently, Applicants respectfully urge that the rejection of claims 9-18 has been overcome.

Furthermore, *Monzel* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. *Monzel* actually teaches away from the presently claimed invention because it teaches using a portion of the array of programmable cells as the peripheral interface logic to access the memory core as opposed to providing a distinct plurality of memory interface control blocks to access the memory cells as in the presently claimed invention. Absent the examiner pointing out some teaching or incentive to implement providing a plurality of memory interface control blocks, one of ordinary skill in the art would

not be led to modify *Monzel* to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify *Monzel* in this manner, the presently claimed invention can be reached only through an improper use of hindsight using Applicants' disclosure as a template to make the necessary changes to reach the claimed invention. Therefore, the rejection of claims 1-18 under 35 U.S.C. § 102 has been overcome.

II. Conclusion

It is respectfully urged that the subject application is patentable over *Monzel* and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: February 8, 2006

Respectfully submitted,

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